

## **TRENCH MIS DEVICE WITH REDUCED GATE-TO-DRAIN CAPACITANCE**

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### **ABSTRACT**

10 Trench MIS devices including a thick insulative layer at the bottom of the trench  
are disclosed, along with methods of fabricating such devices. An exemplary trench  
MOSFET embodiment includes a thick oxide layer at the bottom of the trench, with no  
appreciable change in stress in the substrate along the trench bottom. The thick insulative  
layer separates the trench gate from the drain region at the bottom of the trench yielding a  
15 reduced gate-to-drain capacitance making such MOSFETs suitable for high frequency  
applications. In an exemplary fabrication process embodiment, the thick insulative layer  
is deposited on the bottom of the trench. A thin insulative gate dielectric is formed on the  
exposed sidewall and is coupled to the thick insulative layer. A gate is formed in the  
remaining trench volume. The process is completed with body and source implants,  
passivation, and metallization.

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